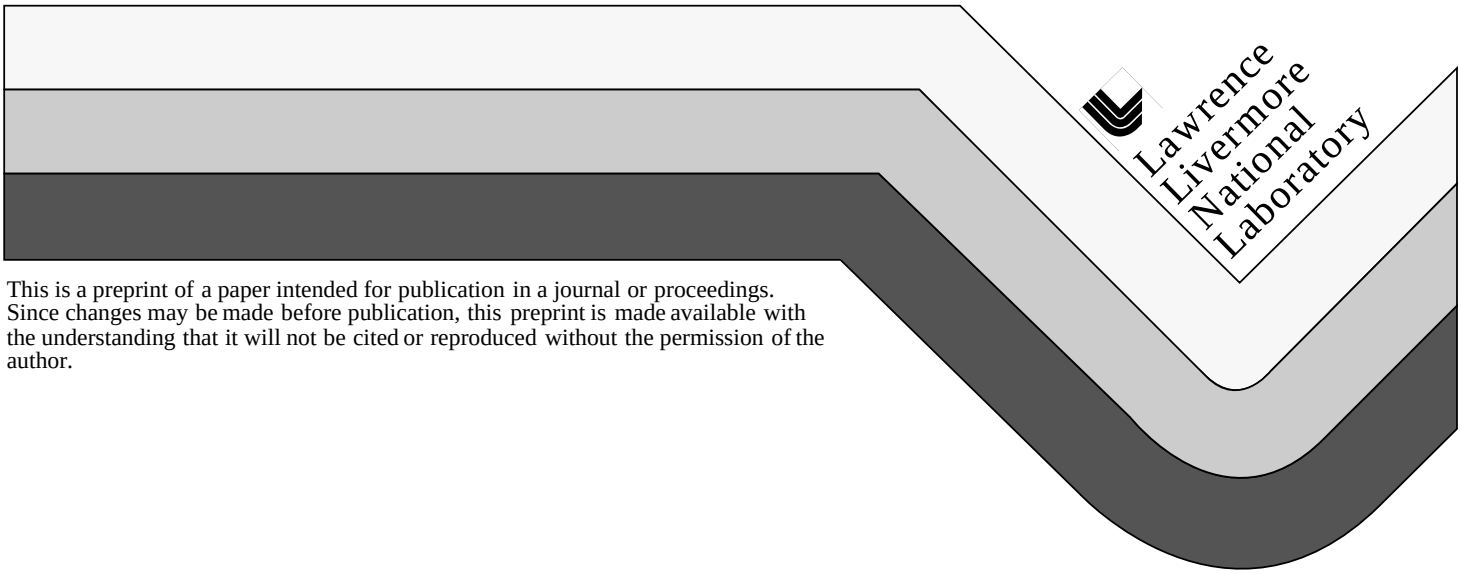
UCRL-JC-132316
PREPRINT

High Energy Density Capacitors Fabricated by Thin Film Technology

Andrew V. Wagner
Gary W. Johnson
Troy W. Barbee Jr

This paper was prepared for submittal to the
Materials Research Society 1999 Spring Meeting
San Francisco, CA
April 4-9, 1999

March 30, 1999



HIGH ENERGY DENSITY CAPACITORS FABRICATED BY THIN FILM TECHNOLOGY

ANDREW V. WAGNER, GARY W. JOHNSON, TROY W. BARBEE JR.
Chemistry and Materials Science Department, Lawrence Livermore National Laboratory
7000 East Avenue, Livermore, CA 94550 USA

ABSTRACT

Low energy density in conventional capacitors severely limits efforts to miniaturize power electronics and imposes design limitations on electronics in general. We have successfully applied physical vapor deposition technology to greatly increase capacitor energy density. The high dielectric breakdown strength we have achieved in alumina thin films allows high energy density to be achieved with this moderately low dielectric constant material. The small temperature dependence of the dielectric constant, and the high reliability, high resistivity, and low dielectric loss of Al_2O_3, make it even more appealing. We have constructed single dielectric layer thin film capacitors and shown that they can be stacked to form multilayered structures with no loss in yield for a given capacitance. Control of film growth morphology is critical for achieving the smooth, high quality interfaces between metal and dielectric necessary for device operation at high electric fields. Most importantly, high rate deposition with extremely low particle generation is essential for achieving high energy storage at a reasonable cost. This has been achieved by reactive magnetron sputtering in which the reaction to form the dielectric oxide has been confined to the deposition surface. By this technique we have achieved a yield of over 50% for 1 cm^2 devices with an energy density of 14 J per cubic centimeter of Al_2O_3 dielectric material in 1.2 kV, 4 nF devices. By further reducing defect density and increasing the dielectric constant of the material, we will be able to increase capacitance and construct high energy density devices to meet the requirements of applications in power electronics.

INTRODUCTION

The continuing miniaturization of power electronics demands further increases in energy storage density in capacitors. Applications such as switching power supplies, high frequency filter capacitors, variable speed electric motors, and pulsed power sources demand low loss, low inductance capacitors that tolerate high temperature.

Nanostructure multilayer capacitors with interleaved films of conductor and dielectric make it possible to pack many thin dielectric layers in parallel. The key to achieving high energy density is making a dielectric layer that can support a very high field strength, since the energy density of the capacitor is proportional to the square of the field strength. To realize the high field strength of materials in a device, it is necessary to make large-area, defect free films, since any defect will lower the voltage at which the device will fail. While the electronics industry continues to develop multilayer ceramic capacitors by powder processing of ferroelectric materials we take a different approach and grow high quality insulators by physical vapor deposition.

The aluminum oxide films discussed here are all made by reactive magnetron sputtering. The dielectric constant of Al_2O_3 is about 9 which is over twice that of silicon dioxide. Like SiO_2, Al_2O_3 deposits as an amorphous film. This eliminates the possibility of through film columnar grain boundaries becoming a breakdown pathway. Also polycrystalline films are more difficult to keep smooth during deposition, and roughness at the interface between the dielectric and the contact can lead to field intensification and breakdown.

Although ferroelectric materials have a much higher dielectric constant and are receiving much attention in the literature, there a number a of reasons we have chosen not to work with them. First, ferroelectric materials must be crystalline to achieve high dielectric constant.

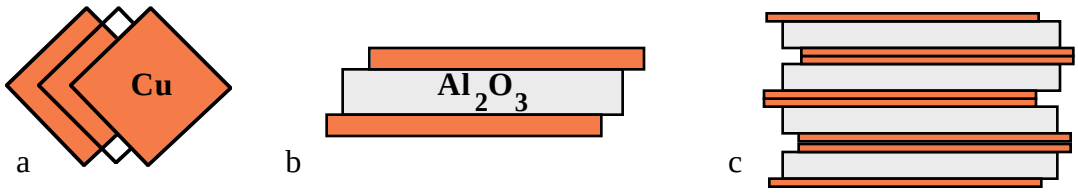


Figure 1: a) Schematic top view of a Cu / Al_2O_3 / Cu capacitor structure deposited though a diamond shaped shadow mask aperture. With this shape one mask can be used to deposit dielectric and contacts allowing the whole capacitor to be deposited without breaking vacuum. b) Cross section of a single layer capacitor. c) The single layer subunit can be repeated to form a multiple layer, stacked capacitor. (Vertical exaggeration 1000x.)

Second, ferroelectric materials have a large piezoelectric effect leading to fatigue and high losses. Finally, the high dielectric constant of ferroelectric materials saturates at high field lowering their potential energy storage density.

The primary goal of this work is to develop an efficient high rate sputtering process for depositing thin film capacitors, while meeting the stringent quality requirements necessary to achieve high capacitance and high energy density. The primary challenges include making fully oxidized very high resistivity films keeping the deposition region particle free to eliminate defects in the films and maintaining smooth and abrupt interfaces with the capacitor contacts.

EXPERIMENTAL PROCEDURE

A small clean room has been constructed around the magnetron sputter deposition system since particle control is crucial. This allows the substrates to be loaded without particle contamination of the substrate or the system. Careful attention is also paid to cleaning the substrate and system parts and preventing deposited materials from flaking off of the chamber walls.

The dielectric films are deposited in a reactive magnetron sputtering system. The sputtering chamber is both a cryo and turbo pumped reaching a base vacuum in the mid 10^{-7} torr. The mechanical roughing and backing pumps are all oil free eliminating possible hydrocarbon contamination of the films. The chamber has three magnetron sputtering sources one for the contact material, a second for reactivity sputtering the dielectric material and a third available for interface modification. The Al sputtering target used to deposit Al_2O_3 is surrounded by an Ar distribution ring which jets high purity Ar in front of the target. The aperture in this ring allows sputtered Al atoms to reach the sample, but the flow of Ar through the aperture limits the amount of oxygen introduced around the sample from diffusing back toward the sputtering target. An additional magnetron sputtering source is available in the chamber. It can be used to modify the interface between the dielectric material and the contact. Cu has been chosen for the contacts because of its high electrical conductivity and our experience growing smooth Cu films.

The capacitors are formed using a diamond shaped shadow mask. The mask has a series of apertures allowing multiple capacitors to be deposited at the same time. The substrate can be shuttled back and forth behind the mask as the substrate and mask rotate toward different sources allowing the layers of metal and dielectric to be deposited to build up the capacitor structure without breaking vacuum. The procedure for constructing a simple capacitor structure is illustrated in figure 1. On top of the capacitor a capping dielectric layer is typically deposited directly over all the other dielectric layers. This protects the top contact and helps prevent flash over between the contacts. Typical substrates are 4 x 7 inch, flame-polished AF 45 glass sheets. For conducting substrates such as Si a different procedure is used. In this case a dielectric film is deposited over the whole surface of the substrate. Then the chamber is vented and the mask installed, before the top contacts can be deposited. This technique does not lend itself to making multiple layer capacitors but does allow the sample to be deposited on Si substrates which can be bought with a well-characterized, clean surface. For samples deposited on high conductivity Si wafers, crude electrical contact is made to the back or edge of the wafer.

Routine electrical measurements include capacitance, dissipation, high field leakage, and capacitor breakdown. The measurements not only relate directly to our development goals but also serve as extremely sensitive, materials characterization tools. For example, measuring leakage current at high electric field is a sensitive indicator of stoichiometry since high leakage current occurs if the film is not fully oxidized.

RESULTS AND DISCUSSION

The sputter deposited Al_2O_3 has been shown to be fully amorphous by x-ray diffraction. TEM observations confirm this and show the structure of the interface between the contact and the dielectric (figure 2). In the device shown in figure 2 the interface between the Cu contact and the dielectric has been modified by adding a 270Å layer of a second metal at the interface. This can be used to modify electrical properties, such as work function, or physical properties, such as interdiffusion. A small amount of roughness has developed at the top of the 1μ thick crystalline Cu bottom contact, but depositing the amorphous Al_2O_3 smoothes out the structure allowing multilayed structures to be grown without propagating roughness.

While TEM provides visualization of the local interface structure it is not suitable for investigating the very low defect density which dominates device performance. To determine defect density caused by particle contamination occurring during deposition, we look at the breakdown strength of capacitors. A histogram of the breakdown field strength for a series of capacitors is shown in figure 3. The capacitors in this data set are of two different areas. Careful examination shows that the larger area capacitors have a lower average breakdown strength than the small capacitors. This can be attributed to the effect of a random distribution of defects in the dielectric films associated with particle contamination. The yield curve for a particular capacitor area can be calculating by integrating the breakdown histogram. Figure 4 shows the yield curves calculated from the two capacitor histograms shown in figure 3, as well as data from larger devices. From the yield curves it is clear that larger devices have lower yield. A simple argument for the decrease in yield with area can be given as follows. The probability of making a capacitor

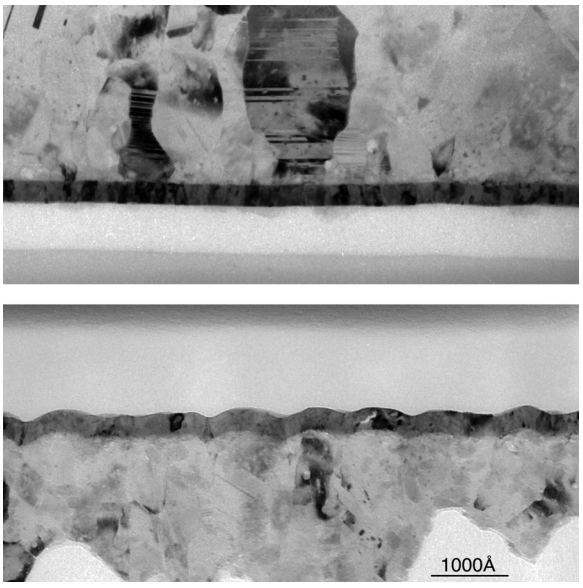


Figure 2: Composite TEM micrograph showing the interface regions between metal and dielectric. (Growth direction up.) Thickness variations associated with sample thinning are visible in the amorphous Al_2O_3 layer. The Cu contacts and a 270Å layer of a second metal at the interface are crystalline.

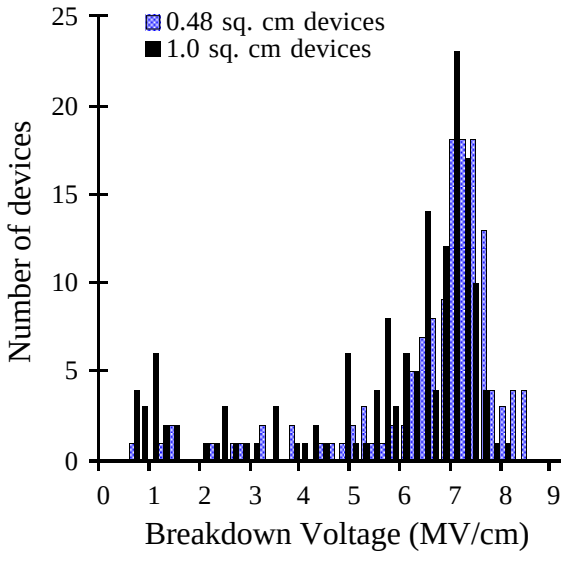


Figure 3: Histogram of the breakdown strength of two different size devices.

which does not break down when tested to a particular field strength is the same as the probability of independently making two capacitors of half the area which survive testing to the same field. Thus, doubling the area of the capacitor squares the yield probability. This can be generalized to say that the yield is a function of the power of the capacitor area. This can be demonstrated experimentally by using a curve based on the yield for a 1 cm^2 device and generating a family of curves for the different area devices as shown in figure 4. It can be seen that the measured yield decreases as the power of the dielectric area for both single and multilayer devices where the device area is the sum of the areas of all the layers.

In figure 5 we show that we have improved capacitor yield over time. The improvement in yield during 1997 can be primarily attributed to improvements in the isolation of the Al target from the reactive oxygen gas caused by using an Ar distribution ring which jets Ar in front of the Al sputtering source. This allows the target to be sputtered with little surface oxide forming on the target (metal mode sputtering) which is important for several reasons. First, the rate is about an order of magnitude higher than when the surface of the target becomes oxidized. This allows us to deposit at typical rates of 10 to 20Å/sec. Second, this means that material depositing on the aperture ring and other areas away from the sample is conducting, which reduces the potential for charge build up and arcing. Finally it means that most of the Al atoms reaching the substrate are metal atoms not metal oxide clusters. This is thought to have a profound effect on the deposition, allowing the energy associated with the oxidation of the Al to be deposited at the growth surface. This technique has been pioneered for SiO_2, and a technique for determining sticking coefficient for oxygen during growth has been developed [1].

The big jump in yield seen in 1998 can be attributed primarily to switching from 20 kHz pulsed DC sputtering to RF sputtering. At 20 kHz the pulse frequency appears to be too low to discharge any oxide which does form on the target or other parts near the gun, for example when the system is vented, and can lead to a low level arcing problem [2]. RF sputtering at 13.6 MHz is able to overcome this problem, and the number of particles visible on the surface decreased as the yield increased.

Reaching full oxidation of the films without oxidizing the target is one of the major challenges. If the target is sufficiently isolated, the oxygen flow can be increased until the film is

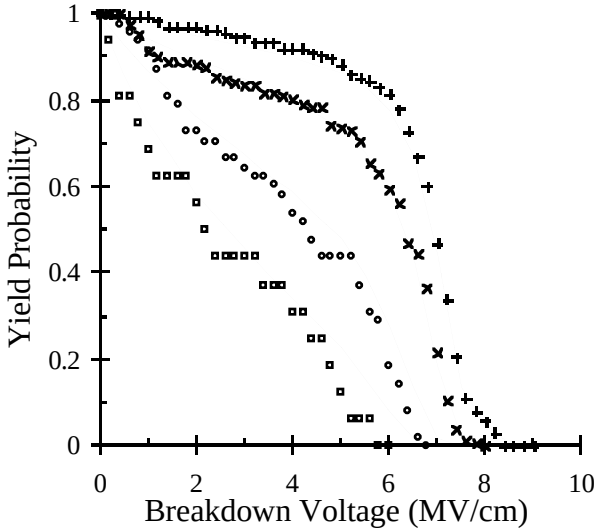


Figure 4: Yield curve for 4 different area devices. 0.48 cm^2 (+), 1.0 cm^2 (x), 2.4 cm^2 (o), two dielectric layer device with each layer 2.4 cm^2 (□). The family of solid curves are formed by taking a yield curve based on the 1 cm^2 device to the power of each device area.

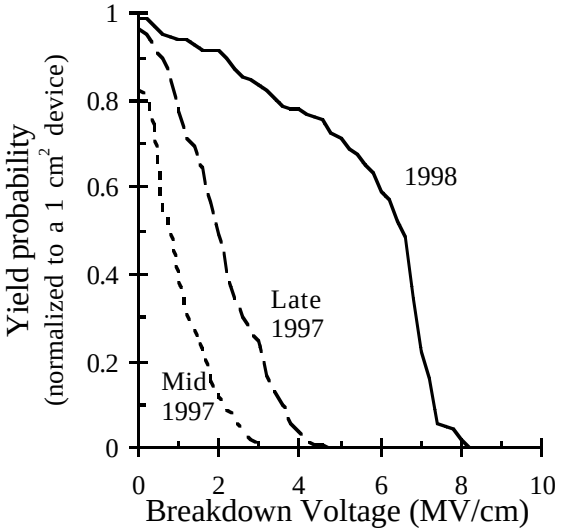


Figure 5: Capacitor yield has improved dramatically since mid 1997 as a result of improved isolation of the magnetron source from the reactive gas and switching to RF sputtering.

fully oxidized without the rate dropping from oxidation of the target. Although clear films are often taken as fully oxidized we find that sufficient oxygen flow to produce highly insulating films is roughly 25% more than that needed to produce completely clear films.

The leakage current in a device with fully oxidized dielectric is shown in figure 6. It can be seen that the current measured at a particular applied voltage is not constant in time. The initial RC time constant of the circuit was 0.07 sec, so the observed current after the first data point can not be attributed to charging of the capacitor itself. After the capacitor has been charged for thousands of seconds, the leakage drops to a very low level. The value of the resistivity of the dielectric at 800 volts and 5000 seconds after applying the field is 3.5×10^{17} Ωcm and still increasing. This resistivity is nearly that of single crystal Al_2O_3 and demonstrates that we have fully oxidized material. The current is found to fall off as 1/t. This is not unusual for dielectric materials. For SiO_2 films used for semiconductor devices a similar behavior has been seen at short times and attributed to tunneling of charge between the contacts and defect states in the dielectric [3]. When the capacitor is shorted the charge which leaked in leaks back out which is consistent with the idea of charge moving between states in the dielectric [4]. It can be seen in figure 7 that at high field the current increases approximately exponentially with field, while at low field current must go to zero. This is consistent with an activated process, for example tunneling, where there are two defect states with a barrier between them. Charge carriers can move between the states with an exponential dependence of the transition probability on barrier height. Applying a bias decreases the barrier for charge carriers jumping forward, while it increases the barrier in the reverse direction. Thus the current I can be written as:

$$I \propto \frac{1}{t} e^{-(U+bV)} - e^{-(U-bV)} \tag{1}$$

$$I = \frac{a}{t} \sinh(bV) \tag{2}$$

Where V is the applied field and U the barrier height between states. Equation 2 with two fitting parameters a and b is in good agreement with the observed field and time dependence of the leakage current as shown in figure 7. This form of the leakage behavior is not unique to a

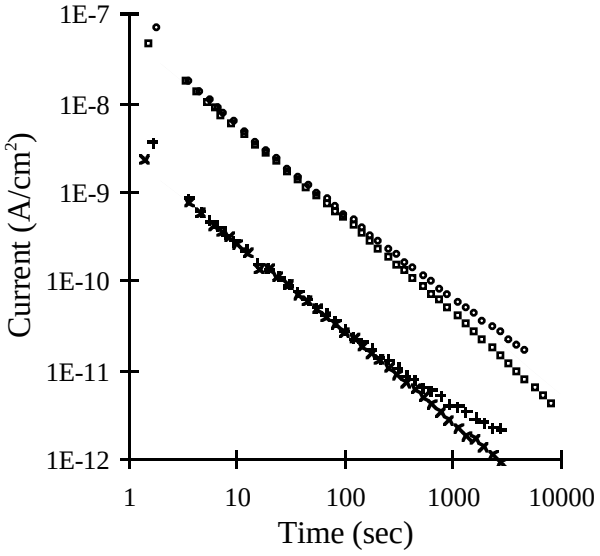


Figure 6: Leakage current as a function of time for two different applied voltages. 50V (0.22 MV/cm) (+), discharging after 50V (x), 800V (3.5 MV/cm) (o), discharging after 800V (□). The lines are a 1/t fit.

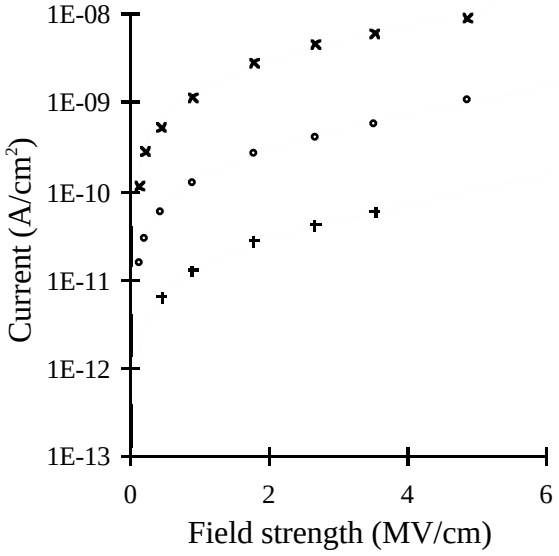


Figure 7: Leakage as a function of field for three different times. 10 sec (x), 100 sec (o) and 1000 sec (+) after the field is applied. The solid lines are a fit to equation 2.

tunneling mechanism. For example, resistive charging at the tapered edges of the contacts would form a RC network which would also give a 1/t dependence of the leakage current [5].

We typically produce capacitors made for 1 kV operation that are designed to survive breakdown testing to 1.2 kV. It can be seen from the yield curve (figure 3) that for a 1 cm^2 device we have a 50% yield at a field of just over 6 MV/cm. To reach 1.2 kV at a field of 6 MV/cm the device must have a dielectric thickness of 2 μ. Such a device has a capacitance of 4 nF and an energy density in the dielectric of 14 J/cm^3 at 1.2 kV. Capacitors at the high end of the yield curve which survive to field strengths of 8 MV/cm reach the very high energy density of 25 J/cm^3 in the dielectric layer. The measured dissipation for the capacitor is typically about 1%, where much of this comes from the contact geometry and not from the dielectric itself. Typically we work with device with area ranging from 0.3 cm^2 to 7.5 cm^2 and dielectric film thickness from 2 to 5 μ. Our largest device to reach 1 kV has an area of 32 cm^2 and a capacitance of 142 nF.

CONCLUSIONS

We have developed a process using reactive, magnetron, sputter deposition to grow thin film capacitors with high energy density in the dielectric layer. Amorphous Al_2O_3 thin films were grown by reactive magnetron sputtering from an Al sputtering target at the high rate associated with an unoxidized target. These films are fully oxidized as deposited and have extremely low DC leakage. The time and voltage dependence of the leakage current in these films follows a simple equation which is consistent with tunneling models discussed in the literature.

We have achieved a continued improvement in yield in our thin film capacitors over the last two years by continuing to decrease the defect levels in sputter deposited films. This has been achieved primarily by improving the sputtering target isolation from the reactive oxygen gas and by minimizing the impact of any small amount of oxygen reaching the target by using RF sputtering. We have given a simple model for understanding yield as a function of area, which we show agrees well with the data. This model can be used to predict what capacitance we can achieve with reasonable yield for a particular level of particle control. By further reducing defect density and using higher dielectric constant materials we will be able to continue increasing capacitance. High energy density devices made by thin film, multilayer techniques promise to meet the demanding requirements of applications in power electronics such as snubber and filter capacitors for electric vehicles.

ACKNOWLEDGMENTS

Funding for this project was provided by the U.S. Department of Energy, Office of Advanced Automotive Technology (DOE-OAAT). We gratefully acknowledge Mark Wall for TEM analysis. This work was done under the auspices of the U.S. DOE by Lawrence Livermore National Laboratory under Contract No. W-7405-Eng-48.

REFERENCES

1. T.W. Barbee Jr., D.L. Keith, L. Nagel, and W.A. Tiller, J. Electrochem. Soc. **131**, 434 (1994).
2. S. Schiller, K.Goedicke, J. Reschke, V. Kirchhoff, S. Schneider, and F. Milde, Surface and Coating Technology, **61**, 331 (1993).
3. T.R. Oldham, A.J. Lelis and F.B. Mclean, IEEE Trans. on Nuclear Science, **NS-33**, 1203 (1986).
4. D.J. Dumin, J.R. Maddux, R.S. Scott, and R. Subramoniam, IEEE Tran. on Electron Devices, **41**, 1570 (1994).
5. R.S. Scott and D.J. Dumin, J. Electrochem. Soc., **142**, 586 (1995)
6. A.K. Jonscher, *Dielectric Relaxation in Solids*, Chelsea Dielectrics Press, London 1983.